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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,757	08/25/2003	Satoshi Yamamoto	241785US2X	1266

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EXAMINER

GEORGE, PATRICIA ANN

ART UNIT PAPER NUMBER

1765

DATE MAILED: 07/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/646,757

Applicant(s)

YAMAMOTO ET AL.

Examiner

Patricia A. George

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08/25/03.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 8/25/2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Drawings

Figures 1, 2A, 2B, and 2C should be designated by a legend such as --Prior Art-- because only that which is old (i.e. "conventional") is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims are rejected under 35 U.S.C. 112, second paragraph,

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Regarding claims 1-3 and 7, and all claims directly or indirectly dependent on them, the phrase "small hole" renders these claims indefinite. See MPEP § 2173.05(d). The term "small hole" is a relative term, not defined by the claim, and the specification does not provide a standard for ascertaining the requisite degree "small hole". One of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The term "small" may be simply deleted.

Regarding claims 1, 2, 4, 6, and 8, and all claims directly or indirectly dependent on them, the phrase "thin metal" renders these claims indefinite. See MPEP § 2173.05(d). The term "thin metal" is a relative term, not defined by the claim, and the specification does not provide a standard for ascertaining the requisite degree "thin metal". One of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The term "thin" may be simply deleted.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1-2 and 5-6 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Noma et al (US Patent No. 6,864,172).

Noma discloses a method of manufacturing a semiconductor substrate provided with a through hole electrode by which first and second principal sides of said semiconductor substrate communicate with each other, said manufacturing method comprising: (a) forming a first insulating layer (Fig. 12A, part 103) on a first principal side (top of 101) of said semiconductor substrate (101); (b) forming a small hole (Fig. 12B, part 114) through said semiconductor substrate extending from the second principal side of said semiconductor substrate (bottom of 101) and to said first insulating layer (103, also, see col. 4, lines 54-57); (c) forming a second insulating layer (Fig. 13A, part 115) on the inside surface of said small hole; (d) forming a thin metal film (see Fig. 10B, parts 106,102,105 and col. 3, lines 26-27) on said first insulating layer; (e) removing a portion of said first insulating layer between said thin metal film and said small hole in order to expose said thin metal film to said small hole (see two step etch process: col. 7, lines 34-38); and (f) filling a conductive material (117) into said small hole in order to form a through hole electrode (Fig. 13B) which is electrically connected to said thin metal film.

As to Claim 2, Noma discloses the manufacturing method of a semiconductor substrate wherein said thin metal film (102/106/105) includes two layers made of different metals. See material types cited col. 6, lines 19-20 and 36.

As to claim 5, Noma discloses (the manufacturing method of a semiconductor substrate wherein) a device that is formed in said first principal side (101) of said semiconductor substrate and that a second insulating layer (113) is further formed in the

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second principal side of said semiconductor substrate. Alternatively, Noma discloses forming another device referred to as an interconnect (Fig. 15A), or that a device 120 is formed in the first principal side (stacking in Fig. 16).

As to claim 6, Noma discloses the manufacturing method of a semiconductor substrate wherein said thin metal film (102/106/105) includes two layers made of different metals. See material types cited col. 6, lines 19-20 and 36-105.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

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Claims 3-4 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noma et al (US Patent No. 6,864,172) in view of Laermer (US Patent No. 5,501,893). The discussion of Noma from above is repeated here.

As to claim 3, Noma fails to disclose DRIE. Noma discloses to use etching (col. 7, lines 34-35) but not the type of etching. Laermer teaches a useful method for etching small holes using DRIE. The advantage of using Laermer's method is a high etch rate with high selectivity when etching silicon with various masks (see col. 6 lines 35-36), which is subsequently known as DRIE.

It would have been obvious to one of ordinary skill in the art to use DRIE as taught by Laermer in the method of Noma because Laermer teaches that it has a high etch rate with high selectivity. It is noted that the manufacturing method forming a hole by Deep-Reactive Ion Etching technique, has become widely used in the semiconductor industry and would be recognized as general state of knowledge.

As to claim 4, see the rejection of claim 2.

As to claim 7, see the rejection of claim 3.

As to claim 8, see the rejection of claim 2.

Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noma et al (US Patent No. 6,864,172). The discussion of Noma from above is repeated here.

As to claim 9, Noma discloses an order of manufacturing (a), (d), (b), (e), (c), and (f). Noma fails to disclose the order of (a), (b), (c), (d), (e), and (f). It would be obvious to one of ordinary skill in the art to use the cited order because of same final product results. (MPEP 2144.04.IV.C, p.157) In re Burhans, 154 F.2d 690, 69 USPQ (selection

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of any order of performing process steps is prima facie obvious in the absence of new or unexpected results).

As to claim 10, Noma discloses an order of manufacturing (a), (d), (b), (e), (c), and (f) in which (e) and (c) are in a different order from that cited. Noma fails to disclose the order of (a), (d), (b), (c), (e), and (f). Noma also fails to disclose the method used for etching. It would be obvious to one of ordinary skill in the art to conduct step (c) before step (e) in the method of Noma, because it would reduce cycle time, and save money, by conducting the oxidation steps together.

As to claim 11, Noma discloses to form an insulating layer on the second principal side of the substrate, but fails to disclose its deposition at step (a). Rather, Noma discloses to form it after step (a). It would have been obvious to one with ordinary skill in the art to deposit the insulative layer at step (a) in the method of Noma in order to protect the new surface during subsequent processing.

As to claim 12, Noma discloses to form an insulating layer on the second principal side of the substrate, but at the step (c) fails to disclose its deposition. It would have been obvious to one with ordinary skill in the art to deposit the insulative layer at step (c) in the method of Noma as it allows the formation of an insulating layer to be formed on the through hole sidewalls at the same time the deposition is being preformed, thus reducing cycle time, a major manufacturing cost contributor.

Further, as to claims 9-12, it would be obvious to one of ordinary skill in the art to use the cited order to obtain the same final product results, see also (MPEP 2144.04.IV.C, p.157) In re Burhans, 154 F.2d 690, 69 USPQ (selection of any order of

performing process steps is prima facie obvious in the absence of new or unexpected results).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

In US Patent 6,790,775, Fartash discloses the method of fabricating a through-substrate interconnect for a microelectronics device. All features of the device in this application are present, including the metal pad. The only difference is that the etch stop of the hole is at the metal, not in/on the top insulator layer.

In US Patent 6,756,681, Hawawa discloses a method for forming a three dimensional integrated circuit stacked structure. The only feature missing is a metal pad on top of the metal filled electrode.

In US Patent 6,239,495, Sakui et al disclose a multi-chip semiconductor device which has a through hole electrode, with insulated sidewalls, located under a metal pad used in conjunction with a ball to make up the stacking configuration.

In US Patent 6,856,210, Zhu et al disclose a multi circuit substrate with a via hole for connecting between circuit layers. This device includes a device built into the substrate in addition to the through hole electrode and both are connected via a vertical metal connector.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571)272-5955. The examiner can normally be reached on Mon. – Fri., 7:00am to 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571)272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



PAG
10 May 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER

